

<b>Notice of Allowability</b>	Application No.	Applicant(s)	
	10/679,467	HANAOKA, TERUNAO	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- **The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1.  This communication is responsive to 7/14/06.
2.  The allowed claim(s) is/are 11-20 and 23-27.
3.  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a)  All
  - b)  Some\*
  - c)  None
 of the:
  1.  Certified copies of the priority documents have been received.
  2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3.  Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4.  A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5.  CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
  - (a)  including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
    - 1)  hereto or 2)  to Paper No./Mail Date \_\_\_\_\_.
  - (b)  including changes required by the attached Examiner's Amendment / Comment or in the Office action of
 Paper No./Mail Date \_\_\_\_\_.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6.  DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1.  Notice of References Cited (PTO-892)
2.  Notice of Draftsperson's Patent Drawing Review (PTO-948) \_\_\_\_\_.
3.  Information Disclosure Statements (PTO/SB/08),  
Paper No./Mail Date \_\_\_\_\_.
4.  Examiner's Comment Regarding Requirement for Deposit  
of Biological Material
5.  Notice of Informal Patent Application
6.  Interview Summary (PTO-413),  
Paper No./Mail Date \_\_\_\_\_.
7.  Examiner's Amendment/Comment
8.  Examiner's Statement of Reasons for Allowance
9.  Other \_\_\_\_\_.

**DETAILED ACTION**

***Allowable Subject Matter***

1. Claims 11-20, and 23-27 are allowed.
2. The following is an examiner's statement of reasons for allowance:

The prior art of record and to the examiner's knowledge does not teach or render obvious, at least to the skilled artisan, the instant invention regarding:

A method of manufacturing a semiconductor device comprising the steps of: forming a redistribution layer (wiring pattern) over a semiconductor wafer which includes an integrated circuit; an interconnect electrically connected with the integrated circuit, and a pad of the interconnect is electrically connected with the redistribution layer (wiring pattern); forming an external terminal on the second section of the redistribution layer (wiring pattern); forming a first resin layer on the redistribution layer (wiring pattern); forming a second resin layer over the first resin layer and in direct contact with the semiconductor wafer so as to cover the side surface of the first resin layer, wherein the first and second resin layers having no wiring therebetween; and cutting the semiconductor wafer, as recited in claims 11 and 23. Claims 12-20, and 25 are dependent upon independent claim 11, and claim 24 is dependent upon independent claim 23.

A method of manufacturing a semiconductor device comprising the steps of: forming a redistribution layer (wiring pattern) over a semiconductor wafer with a passivation film formed thereon, the semiconductor wafer includes an integrated circuit, an interconnect electrically connected with the integrated circuit, and a pad of the interconnect is electrically connected with the redistribution layer (wiring pattern); forming an external terminal on the second section of

the redistribution layer (wiring pattern); forming a first resin layer on the passivation film and at least a part of the first resin layer is placed on the redistribution layer (wiring pattern); forming a second resin layer over the first resin layer and in direct contact with the passivation film so as to cover the side surface of the first resin layer, wherein the first and second resin layers having no wiring therebetween; and cutting the semiconductor wafer, as recited in claims 26 and 27.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

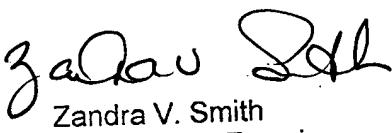
**Contact Information**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

  
Zandra V. Smith  
Supervisory Patent Examiner

23 Sept. 2004